CLAIMS

1. A method of forming semiconductor circuitry, comprising:

providing a monocrystalline silicon substrate;

forming a mask which covers a first portion of the substrate and leaves a second portion uncovered;

forming a recess in the uncovered portion;

at least partially filling the recess with a semiconductive material that comprises at least 1 atomic percent of an element other than silicon;

removing the mask;

forming a first semiconductor circuit component over the first portion of the substrate; and

forming a second semiconductor circuit component over the semiconductive material that at least partially fills the recess.

2. The method of claim 1 wherein the substrate comprises a monocrystalline silicon wafer, and wherein the recess is formed within the monocrystalline silicon of the wafer.

3. The method of claim 1 wherein the substrate comprises a monocrystalline silicon mass over an insulative material, and wherein the recess is formed within the monocrystalline silicon mass.

4. The method of claim 1 wherein the substrate comprises a bulk monocrystalline silicon structure, an insulative material over the bulk monocrystalline structure, and a monocrystalline silicon mass over the insulative material, and wherein the recess is formed through the monocrystalline silicon mass and to the insulative material.

5. The method of claim 1 wherein the substrate comprises a bulk monocrystalline silicon structure, an insulative material over the bulk monocrystalline structure, and a monocrystalline silicon mass over the insulative material, and wherein the recess is formed through the monocrystalline silicon mass and insulative material, and to the bulk monocrystalline structure.

6. The method of claim 1 wherein the semiconductive material that at least partially fills the recess comprises a III/V compound semiconductive material.

7. The method of claim 1 wherein the semiconductive material that at least partially fills the recess comprises silicon and at least 1% carbon.

8. The method of claim 1 wherein the semiconductive material that at least partially fills the recess consists essentially of silicon and at least 1% carbon.

9. The method of claim 1 wherein the semiconductive material that at least partially fills the recess consists of silicon and at least 1% carbon.

10. The method of claim 1 wherein the semiconductive material that at least partially fills the recess consists essentially of a III/V compound semiconductive material.

11. The method of claim 1 wherein the semiconductive material that at least partially fills the recess comprises Si and Ge, with the Ge being present to an atomic concentration of from about 1% to about 20%.

12. The method of claim 1 wherein the semiconductive material that at least partially fills the recess consists essentially of Si and Ge, with the Ge being present to an atomic concentration of from about 1% to about 20%.

13. The method of claim 1 further comprising, before at least partially filling the recess with the semiconductive material, providing an insulative material spacer along a sidewall of the recess; and wherein the at least partially filling the recess with the semiconductive material comprises providing the semiconductive material along the insulative material spacer.

14. The method of claim 13 wherein the insulative material comprises silicon nitride.

15. The method of claim 13 wherein the insulative material comprises silicon dioxide.

16. A method of forming semiconductor circuitry, comprising:

providing a substrate comprising a first monocrystalline material, an insulative layer over the first monocrystalline material, and a second monocrystalline material over the insulative layer and spaced from the first monocrystalline material by at least the insulative layer; the second monocrystalline material consisting essentially of a first element;

forming a mask to cover a first portion of the second monocrystalline material, while leaving a second portion uncovered;

removing at least some of the uncovered portion to form a recess;

at least partially filling the recess with a semiconductive material that comprises at least 1 atomic percent of an element other than the first element;

removing the mask;

forming a first semiconductor circuit component over the first portion of the second monocrystalline material; and

forming a second semiconductor circuit component over the semiconductive material that at least partially fills the recess.

17. The method of claim 16 wherein the first and second monocrystalline materials consist essentially of silicon.

18. The method of claim 16 wherein the first and second monocrystalline materials consist essentially of silicon, and wherein the insulative layer consists essentially of silicon dioxide.

19. The method of claim 16 wherein the mask comprises a layer consisting essentially of silicon nitride over a layer consisting essentially of silicon dioxide.

20. The method of claim 16 wherein the semiconductive material that at least partially fills the recess comprises silicon and at least 1% carbon.

21. The method of claim 16 wherein the semiconductive material that at least partially fills the recess consists essentially of silicon and at least 1% carbon.

22. The method of claim 16 wherein the semiconductive material that at least partially fills the recess consists of silicon and at least 1% carbon.

23. The method of claim 16 wherein the semiconductive material that at least partially fills the recess comprises a III/V compound semiconductive material.

24. The method of claim 16 wherein the semiconductive material that at least partially fills the recess consists essentially of a III/V compound semiconductive material.

25. The method of claim 16 wherein the semiconductive material that at least partially fills the recess comprises Si and Ge, with the Ge being present to an atomic concentration of from about 1% to about 20%.

26. The method of claim 16 wherein the semiconductive material that at least partially fills the recess consists essentially of Si and Ge, with the Ge being present to an atomic concentration of from about 1% to about 20%.

27. The method of claim 16 wherein the semiconductive material that at least partially fills the recess consists essentially of Si and Ge, with the Ge being present to an atomic concentration of from about 1% to about 20%; the method further comprising exposing the semiconductive material to a laser to anneal the Si and Ge of the semiconductive material.

28. The method of claim 27 wherein the anneal comprises maintaining the semiconductive material at a temperature of from about 800°C to about 1100°C for a time of from about 20 seconds to about 5 minutes, and exposing the semiconductive material to laser light having a wavelength which interacts with one or more components of the semiconductive material.

29. The method of claim 16 wherein the semiconductive material entirely fills the recess; wherein the semiconductive material consists essentially of Si and Ge, with the Ge being present to an atomic concentration of from about 1% to about 20%; and the method further comprising:

chemical-mechanical polishing the semiconductive material to form a planarized surface which extends across the semiconductive material and mask;

after the chemical-mechanical polishing, exposing the semiconductive material to a laser to anneal the Si and Ge of the semiconductive material; and

the removing the mask occurring after the anneal.

30. The method of claim 29 wherein, after the removal of the mask, the semiconductive material extends above an uppermost surface of the first portion of the second monocrystalline substrate by a distance of from about 50Å to about 200Å.

31. A semiconductor construction, comprising:

a bulk semiconductive material structure;

an insulative material over the bulk semiconductive material structure;

a mass of semiconductive material over a first portion of the insulative material and not over a second portion of the insulative material; the semiconductive material of the mass comprising at least 1 atomic percent of an element other than silicon; and

a monocrystalline silicon layer over the second portion of the insulative material.

32. The construction of claim 31 wherein the mass of semiconductive material is physically against the insulative material.

33. The construction of claim 31 wherein the monocrystalline silicon layer has a segment which extends over the first portion of the insulative material, and wherein the mass of semiconductive material is over the segment of the monocrystalline silicon layer.

34. The construction of claim 31 wherein the semiconductive material of the mass comprises silicon and at least 1% carbon.

35. The construction of claim 31 wherein the semiconductive material of the mass consists essentially of silicon and at least 1% carbon.

36. The construction of claim 31 wherein the semiconductive material of the mass consists of silicon and at least 1% carbon.

37. The construction of claim 31 wherein the semiconductive material of the mass comprises a III/V compound semiconductive material.

38. The construction of claim 31 wherein the semiconductive material of the mass consists essentially of a III/V compound semiconductive material.

39. The construction of claim 31 wherein the semiconductive material of the mass comprises Si and Ge, with the Ge being present to an atomic concentration of from about 1% to about 20%.

40. The construction of claim 31 wherein the semiconductive material of the mass consists essentially of Si and Ge, with the Ge being present to an atomic concentration of from about 1% to about 20%.

41. The construction of claim 31 wherein the semiconductive material of the mass has an uppermost surface; wherein the monocrystalline silicon layer has an uppermost surface; and wherein the uppermost surface of the semiconductive material of the mass extends above the uppermost surface of the monocrystalline silicon layer by a distance of from about 50Å to about 200Å.

42. The construction of claim 31 further comprising:

an array of memory devices over the monocrystalline silicon layer and not over the semiconductive material of the mass; and

circuitry peripheral to the array of memory devices over the semiconductive material of the mass.

43. The construction of claim 31 further comprising:

a semiconductor circuit component over the monocrystalline silicon layer and not over the semiconductive material of the mass; and

wherein the semiconductor circuit component corresponds to a transistor of a DRAM cell, and a DRAM cell is not formed over the semiconductive material of the mass.

44. A semiconductor construction, comprising:

a monocrystalline silicon material; and

a mass of semiconductive material over a first portion of the monocrystalline silicon material and not over a second portion of the monocrystalline silicon material; the semiconductive material of the mass comprising at least 1 atomic percent of an element other than silicon.

45. The construction of claim 44 wherein the semiconductive material of the mass comprises silicon and at least 1% carbon.

46. The construction of claim 44 wherein the semiconductive material of the mass consists essentially of silicon and at least 1% carbon.

47. The construction of claim 44 wherein the semiconductive material of the mass consists of silicon and at least 1% carbon.

48. The construction of claim 44 wherein the semiconductive material of the mass comprises a III/V compound semiconductive material.

49. The construction of claim 44 wherein the semiconductive material of the mass consists essentially of a III/V compound semiconductive material.

50. The construction of claim 44 wherein the semiconductive material of the mass comprises Si and Ge, with the Ge being present to an atomic concentration of from about 1% to about 20%.

51. The construction of claim 44 wherein the semiconductive material of the mass consists essentially of Si and Ge, with the Ge being present to an atomic concentration of from about 1% to about 20%.

52. The construction of claim 44 wherein the semiconductive material of the mass has an uppermost surface; wherein the monocrystalline silicon material has an uppermost surface; and wherein the uppermost surface of the semiconductive material of the mass extends above the uppermost surface of the monocrystalline silicon material by a distance of from about 50Å to about 200Å.

53. The construction of claim 44 further comprising:

an array of memory devices over the monocrystalline silicon material and not over the semiconductive material of the mass; and

circuitry peripheral to the array of memory devices over the semiconductive material of the mass.

54. The construction of claim 44 further comprising a spacer between the monocrystalline silicon material and at least some of the mass of semiconductive material.

55. The construction of claim 54 wherein the spacer comprises silicon nitride.

56. The construction of claim 54 wherein the spacer comprises silicon dioxide.